CLAIMS

What is claimed is:

1. An apparatus, comprising:

a first set of address line outputs;

a second set of address line outputs that is a copy of a subset of the first set of address line outputs, the second set of address line outputs including at least 5 address line outputs;

a command-per-clock detection unit to compare a current address with a previous address, the current and previous addresses including a subset of address bits corresponding to the first set of address line outputs less the address bits represented by the second set of address line outputs; and

a chip select output to maintain a chip select line in an asserted state if the command-per-clock detection unit finds a match between the current and previous addresses.

2. The apparatus of claim 1, the first set of address lines including at least address lines [12:0].

3. The apparatus of claim 2, the second set of address lines including a copy of address lines [5:1].

4. The apparatus of claim 3, the command-per-clock detection unit to compare a current address including address bits [12:6,0] with a previous address including address bits [12:6,0].

5. The apparatus of claim 4, further comprising a second command-per-clock detection unit to provide command-per-clock control for a second memory interface.

6. A system, comprising:

a memory controller including

a first set of address line outputs,

a second set of address line outputs that is a copy of a subset of the first set of address line outputs, the second set of address line outputs including at least 5 address line outputs,

a command-per-clock detection unit to compare a current address with a previous address, the current and previous addresses including a subset of address bits corresponding to the first set of address line outputs less the address bits represented by the second set of address line output, and

a chip select output to maintain a chip select line in an asserted state if the command-per-clock detection unit finds a match between the current and previous addresses; and

a memory device coupled to the memory controller via a first and second set of

address lines and the chip select line, the first and second address lines coupled to the first and second address line outputs.

7. The system of claim 6, the first set of address lines including at least address lines [12:0].

8. The system of claim 7, the second set of address lines including a copy of address lines [5:1].

9. The system of claim 8, the command-per-clock detection unit to compare a current address including address bits [12:6,0] with a previous address including address bits [12:6,0].

10. The system of claim 9, wherein the memory device is a DDR memory device.

11. The system of claim 10, further comprising a second memory device coupled to the memory controller.

12. The system of claim 11, the memory controller further including a second command-per-clock detection unit to allow command-per-clock chip select timing for the second memory device.

13. The system of claim 12, wherein the second memory device is a DDR memory device.

14. A method, comprising:

providing copies of at least 5 address lines;

comparing a subset of a current address with a subset of a previous address; and

continuing to assert a chipset select line if there is a match between the subset of the current address with the subset of the previous address.

15. The method of claim 14, further comprising deasserting the chip select line for a clock period if there is no match between the subset of the current address with the subset of the previous address.